Partial Translation of Yamamoto
(Jpn. Pat. Appln. KOKAI Publication No.8-97352)

Page 3, column 4, line 25 to page 5, column 7, line 19

[0016]

[Embodiment]

Next, embodiments of the present invention will be explained by referring to the drawings.

[0017]

FIG. 1 is a cross section of the multi-chip module showing the first embodiment of the present invention, and FIG. 2 (a) is a cross section of the connection pad used for connecting terminals of the peripheral electronic components mounted on the ceramic multilayer wiring cap. FIG. 2 (b) is a cross section of the input/output pin electrically connecting wiring of the substrate for mounting the semiconductor chip and multilayer wiring of the ceramic multilayer wiring cap.

[0018]

FIG. 1 shows the prior art wherein the multi-chip module comprises ceramic multilayer wiring substrate 1 which is baked by laminating green sheets such as alumina, ceramic multilayer wiring cap 2 and heat radiating metal plate 4 on which semiconductor chip 3 is mounted; the ceramic multilayer wiring substrate 1 has a predetermined sized first opening, a second opening which is smaller than the first opening, a third opening which is smaller than the second opening, and a fourth opening which is smaller than the third opening at one surface; and the depth of the openings are determined depending on the number of laminated alumina sheets.

[0019]

The first opening is connected to the ceramic multilayer wiring cap 2, and the second and third openings have bonding pads 5 used for wire bonding between the input/output pads of the semiconductor chip 3 and wiring of the ceramic multilayer wiring substrate.

[0020]

The heat radiating metal plate 4 is externally bonded to the fourth opening by using the prior art brazing technology, and the semiconductor chip 3 is mounted on the heat radiating metal plate 4 on the side of the opening. Further, a predetermined number of input/output pins 7 are fixed on the periphery of the first opening by the prior

art brazing technology. The fixed portions are electrically connected to the bonding pads 5 of the second and third openings via multilayer wiring in the substrate.

[0021]

The ceramic multilayer wiring cap 2 is a multilayer wiring cap made by the same technology used for the ceramic multilayer wiring substrate 1. The input/output pins 7 are inserted in the periphery of the cap 2 connected to the periphery of the first opening of the substrate 1, and the pins 7 have a predetermined number of pin holes for electrical connection between the substrate 1 and the cap 2. Connection pads 13 are provided on the bottoms of the pin holes. The connection pads 13 are electrically connected to multilayer wiring in the ceramic multilayer wiring cap. The depth of the pin holes is determined depending on the length of pin with a stopper. For example, when the whole length of the pin is 3.8 mm, a brim-shaped stopper is provided in the pin at a point 2.8 mm from the end, and the other end of the pin is buried to the ceramic multilayer wiring substrate 1 to the stopper so as to align the heights of pins.

[0022]

Peripheral electronic component 9 is provided on one surface of the ceramic multilayer wiring cap opposed to the first opening of the ceramic multilayer wiring substrate 1, and each of the terminals of the peripheral electronic component 9 is electrically connected to the multilayer wiring provided inside via connection pad 12 provided on the same surface of the cap. Input/output bumps 8 are connected to the reverse surface of the surface on which the electronic component is mounted by the prior art technology. The bumps 8 are electrically connected to a predetermined connection pad 12 and connection pad 13. Conventionally, pins may be used instead of these bumps 8.

[0023]

Heat sink 11 is bonded to the other surface of the heat radiating metal plate 4, and the periphery of the opening of the ceramic multilayer wiring substrate 1 and the periphery of the ceramic multilayer wiring cap 2 are strictly sealed by using a sealing member like solder.

[0024]

It is preferable to use sealing solder as the sealing member, which can seal

with a low temperature and defuse the stress based on the difference of thermal expansion coefficient between the substrate 1 and the cap 2, so as to easily exchange the ceramic multilayer wiring substrate 1 and ceramic multilayer wiring cap 2.

[0025]

The multi-chip module of this embodiment having the above structure can be freely designed relative to the electrical characteristics by changing the number of laminated alumina sheets of the ceramic multilayer wiring cap 2 and inner wiring pattern. That is, tungsten (W) is printed on the surface of the alumina sheets to form an electrical circuit. It is possible to freely change the electrical characteristics of the package (for example, inductance, capacitance, resistance) by changing the electrical circuit pattern and the number of laminated alumina sheets.

[0026]

In the above explanation, we explained the case where one opening in which semiconductor chip 3 is mounted is provided; it is possible to provide a plurality of sets on the same substrate.

[0027]

It is also possible to make whole inner surfaces of the pin holes as pad, instead of providing the connection pad 13 on the bottom surfaces of the pin holes.

[0028]

Further, it is possible to provide the input/output pin 7 on the side of the ceramic multilayer wiring cap 2, and provide the pin holes fitted with the input/output pin on the ceramic multilayer wiring substrate 1.

[0029]

If the inner surface of the pin hole has conductivity, it can be a through hole passing to the reverse surface. If the hole is not a through hole, input/output bumps 8 can be provided like a check pattern on the whole of the reverse surface of the surface on which the electrical component of the ceramic multilayer wiring cap 2 is mounted.

[0030]

In reference to FIG. 3 which shows a cross section of the second embodiment of the present invention, the difference between the multi-chip module and that of the first embodiment is to provide ceramic frame 21 on the surface on which the electrical component of the ceramic multilayer wiring cap 2 is mounted. The other structures are

the same as the first embodiment; the explanation will be omitted.

[0031]

The ceramic frame 21 is formed in such a manner to surround the peripheral electronic component 9 according to the shape of the first opening, and the ceramic frame 21 is bonded by using the prior art brazing technology.

[0032]

Since the ceramic frame 21 is provided, when the ceramic multilayer wiring substrate 1 and ceramic multilayer wiring cap 2 are bonded, the ceramic frame 21 can be used for a jig to determine the bonding position. Therefore, if a plurality of connection pins 7 are provided, the pins are easily inserted into the pin holes.

[0033]

In addition, it is possible to protect the peripheral electrical components mounted on the side of the ceramic multilayer wiring cap 2 from malfunctions such as breakage when the peripheral electrical components are connected to the ceramic multilayer wiring substrate 1.

[0034]

In the above explanation, the ceramic frame 21 is shaped according to the shape of the first opening; however, the frame 21 can be formed as an L-shape or a U-shape (indicated with dotted lines in the figure) if the shape can be used as a jig for position determination.

[0035]

[Advantages]

As explained above, the multi-chip module having the electrical component of the present invention is perforated in the periphery of the ceramic multilayer wiring cap and inserts the input/output pin of the ceramic multilayer wiring substrate into the pin hole having a conductive pad on the inner surface. In such a structure, the electrical connection between the ceramic multilayer wiring cap and ceramic multilayer wiring substrate is ensured. Also, the cap and the substrate are sealed by heat after the input/output pin of the ceramic multilayer wiring cap is inserted into the pin hole of the ceramic multilayer wiring cap, by providing the ceramic frame to reliably insert the pin. It is easy to attach the heat sink since peripheral electrical components are not mounted on space on the surface of the ceramic multilayer substrate, and that

improves the workability of package assembly.

[0036]

In addition, peripheral electrical components of the semiconductor chip are mounted on the ceramic multilayer wiring cap; thus, the space on the surface of ceramic multilayer substrate can be effectively used, and the heat radiating metal plate and heat sink can be freely selected.

[0037]

The input/output terminals can be provided on the whole of the reverse surface of the surface on which peripheral electrical components of the ceramic multilayer wiring cap are provided, and it can be applied to the multi-pin type packages.

[0038]

The ceramic multilayer wiring substrate and the ceramic multilayer wiring cap can be assembled individually; thus, the package assembly processes can be reduced.

[0039]

Furthermore, the low temperature sealing solder is used for bonding the ceramic multilayer wiring substrate and the ceramic multilayer wiring cap; thus, it is easy to exchange them when the peripheral electrical components mounted on the side of the ceramic multilayer wiring cap and the semiconductor chip mounted on the side of ceramic multilayer wiring substrate are broken.